

**ABSTRACT OF THE DISCLOSURE**

An internal bus structure for a multi-processor-bus system. More specifically, an internal bus protocol/structure is described. The internal bus structure includes unidirectional, point-to-point connections between control modules. The individual buses carry unique transactions corresponding to a request. Each transaction includes an identification tag. The present protocol provides for efficient communication between processors, peripheral devices, memory and coherency modules. The present protocol and design scheme is generic in that the techniques are scalable and re-usable.

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